REMARKS

The Examiner is thanked for the Office Action dated December 1, 2004 in which a more detailed explanation of the basis for the rejection is explained.

Applicant has amended the independent claims 1, 10 and 20, of the present case. In addition, Applicant has added new claims 23-25, of which 24 is an independent claim.

New claim 1 has been amended to more particularly point out and distinctly claim the subject matter of the present invention. In particular, claim 1 specifies that the data generator is internal to the integrated circuit. The Examiner noted in the rejection, page 6, paragraph 7 that Applicant had argued the prior art does not have an internal circuit to generate task patterns. The Examiner noted that the features upon which the arguments were based were not recited in the claims. Accordingly, this feature has been placed in claim 1 and represents a distinction over the Ayres reference. Namely, according to the present invention of the data generators internal to the integrated circuit the generating a selected bit pattern to the memory. This feature is distinctly different from the Ayres '461 reference which requires an external data generator as previously discussed.

An additional distinction over the Ayres reference is also clearly present in claim 1, as amended. Claim 1 specifies that the semiconductor integrated circuit includes combinatorial logic components and a testing circuit for testing the combinatorial logic components after the data generator has input the selected bit pattern to the memory. This is a significant distinction over Ayres, and the other prior art cited.

The purpose of the BIST data generator '301 in Ayres is to provide a test pattern to the memory block for the testing of memory. This is not at all the purpose of the data generator in the present invention. The purpose of the data generator of the present invention is to generate a pattern to be written to memory before the testing of other parts of the circuit. The memory is not being tested; it is logic components on the same integrated circuit, other than the memory which is being tested. The bit pattern is written to the memory before the testing of the logic circuits so that the memory is rendered predictable to the surrounding logic circuitry. Once the memory is rendered predictable to the surrounding circuitry, this logic circuitry can be tested

without the testing being influenced by the unpredictable behavior of the memory. This is not a test data pattern for the memory rather, it is a selective pattern to render the memory predictable prior to the logic components to the circuit receiving a test pattern to test the logic components. It is not the memory being tested; it is the logic components being tested.

The Examiner is directed to Figure 12 of the present application in combination with Figure 4. As shown in Figure 12, the RAM or other memory array, with a CAM or EEPROM, is loaded with a test pattern to represent a combinatorial logic model. This is shown as reference number 30 in Figure 12. An explanation and move embodiments are is provided beginning at the bottom of page 11, line 25 and continue on to page 12. Turning now to Figure 4, the memory array has the same reference number 30. Since it is the same component in both figures. The goal of the present invention is to pre-load the memory with a selected bit pattern to cause the memory to function as if it were a logic element. It may, for example simulate a combinatorial logic circuit such as an AND gate an INVERTER of the type shown in Figure 12. Alternatively, it may simulate some other combinatorial logic circuit such as a series of inverters or other logic.

A description of one embodiment the invention is provided on page 5, beginning at line 3, in which it is pointed out that the RAM array 20 has the contents configured prior to testing. A wrapper circuit 40 is provided which permits a selected bit pattern to be loaded into the memory array so that it may simulate a logic element.

As explained on page 6, line 23-29 the function of the wrapper circuit is to allow the memory to operate in a normal mode, or selectively to fill the memory with the test pattern so that the memory acts as a combinatorial logic element when the logic elements are being tested. See additionally, page 8, the last full paragraph which describes how the RAM is affectively turned into a ROM having a predictable combinatory properties, as a further embodiment.

One major problem addressed by the invention is the testing of logic circuitry that has embedded memory adjacent to the logic circuitry. According to the present invention, the memory is rendered to behave as a known combinatorial logic element and is placed in the data path of the other logic elements to be tested. Now, the entire system to be tested with the memory affectively operating as a known logic element in the integrated circuit so that other

portions of the logic circuit namely, those prior to and after the memory in the signal path can be adequately tested to ensure proper operation of the entire integrated circuit.

With the increasing number of complex logic circuits and the large amounts of embedded memory or a single chip, the ability to test logic circuits which have numerous embedded memories, often of different sizes, on the same integrated circuit, is particularly beneficial.

Accordingly, claim 1, as amended, specifying that it includes a testing circuit for testing a combinatorial logic components after the data generator has input the selected bit pattern to the memory is patentable over the art.

Claim 10 as amended is also believed patentable in light of the art. Claim 10 specifies that the circuit further includes a logic testing circuit coupled to the logic elements and configured to test the operation of the logic elements based on the selected bit pattern present in the memory array. This is a feature distinctly different from and not found in the Ayers '461 patent. As previously explained, one principle of the present invention is that the logic elements are tested after the memory has stored therein a selected bit pattern so that the operation of the memory is completely predictable. This permits the logic elements to be tested even though there are one or more memory arrays on the same integrated circuit interacting with the logic.

Claim 20 has also been amended to specify the method steps of inputting selected data into the logic to be tested and transferring signals from the logic to be tested to the memory and from the memory to the logic to test the logic. Claim 20 makes clear that it is the logic being tested and that the memory has been placed in a preselected form so that the output of the memory is known for giving input, thus permitting the logic both before and after the memory to be tested.

New claim 24 is believed patentable in light of the art. New claim 24 specifies the steps of inputting to the memory array a selected pattern of data bits so as to configure the memory array to operate as a combinatorial logic circuit. After this, the steps are followed to set the integrated circuit in logic test mode and then input signals into the logic as part of the testing. The signals input to the logic may also be input to and from the memory array as part of the

circuit being tested to ensure that the interaction between the logic circuit and the memory array is properly configured.

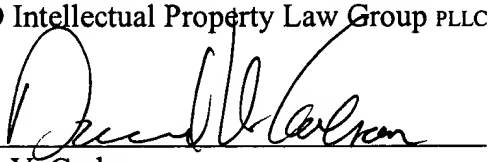
The claims, as now presented are believed clearly patentable in light of the prior art of record and allowance of all claims are respectfully requested.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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